

1. Features

The KXN5610A is the highest performance trench N-ch MOSFETS with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KNX5610A meet the RoHS and green product requirement.

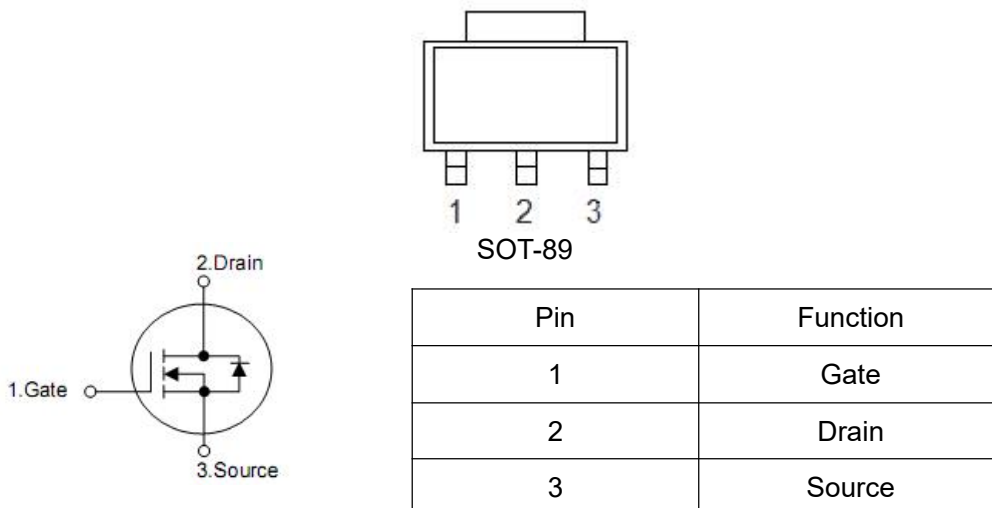
2. Features

- $R_{DS(ON)}=98m\Omega(\text{typ.})@V_{GS}=10V$
- Advanced high cell density trench technology
- Super low gate charge
- Excellent Cdv/dt effect desline
- Green device available

3. Applications

- High frequency point-of-load synchronous buck converter
- Networking DC-DC power system
- Load switch

4.Symbol



Part Number	Package	Brand
KNS5610A	SOT-89	KIA

4. Absolute maximum ratings

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	100	V
Gate-source voltage		V_{GS}	+20	V
Continuous drain current, $V_{GS}@10V$ ¹	$T_C=25^\circ C$	I_D	7*	A
	$T_C=100^\circ C$		5.2	
	$T_A=25^\circ C$		2	
	$T_A=100^\circ C$		1.4	
Pulsed drain current ²		I_{DM}	14	
Power dissipation ³	$T_C=25^\circ C$	P_D	22.7	W
	$T_A=25^\circ C$		2	
Avalanche current		I_{AS}	6	A
Operating junction and storage temperature range		T_J, T_{STG}	-55 to 150	$^\circ C$

* Drain current limited by maximum junction temperature.

5. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance junction-case	$R_{\theta JC}$	-	2.6	$^\circ C/W$
Thermal resistance junction-ambient	$R_{\theta JA}$	-	48	

6. Electrical characteristics

($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	100	-	-	V
BV_{DSS} temperature coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference 25°C $I_D=1\text{mA}$	-	0.098	-	$\text{V}/^{\circ}\text{C}$
Drain-source on-resistance ²	$R_{DS(on)}$	$V_{GS}=10V, I_D=5A$	-	98	115	m Ω
		$V_{GS}=4.5V, I_D=3A$	-	110	125	
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.85	3.0	V
$V_{GS(TH)}$ temperature coefficient	$\Delta V_{GS(TH)}$		-	-4.57	-	$\text{mV}/^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$ $T_J=25^{\circ}\text{C}$	-	-	1	μA
		$V_{DS}=80V, V_{GS}=0V$ $T_J=55^{\circ}\text{C}$	-	-	5	
Gate-source forward leakage	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	± 100	nA
Forward transconductance	g_{fs}	$V_{DS}=5V, I_D=10A$	-	13	-	S
Gate resistance	R_g	$V_{DS}=0V, V_{GS}=0V$ $f=1\text{MHz}$	-	1.8	-	Ω
Total gate charge(10V)	Q_g	$V_{DS}=80V, I_D=10A$ $V_{GS}=10V$	-	26.2	-	nC
Gate-source charge	Q_{gs}		-	4.6	-	
Gate-drain charge	Q_{gd}		-	5.1	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=50V, I_D=10A,$ $R_G=3.3\Omega, V_{GS}=10V$	-	4.2	-	ns
Rise time	t_r		-	8.2	-	
Turn-off delay time	$t_{d(off)}$		-	35.6	-	
Fall time	t_f		-	9.6	-	
Input capacitance	C_{iss}	$V_{DS}=15V, V_{GS}=0V$ $f=1\text{MHz}$	-	1535	-	pF
Output capacitance	C_{oss}		-	60	-	
Reverse transfer capacitance	C_{rss}		-	37	-	
Continuous source current ^{1,6}	I_S	$V_D=V_G=0V,$ Force current	-	-	7	A
Maximum pulsed current ^{2,6}	I_{SM}		-	-	49	
Diode forward voltage ²	V_{SD}	$I_S=1A, V_{GS}=0V$ $T_J=25^{\circ}\text{C}$	-	-	1.3	V
Reverse recovery time	t_{rr}	$I_F=10A, di/dt=100A/\mu s$ $T_J=25^{\circ}\text{C}$	-	37	-	ns
Reverse recovery charge	Q_{rr}		-	27.3	-	nC

Note:

1. The data tested by surface mounted on a 1 inch² board with 20Z copper.
2. The data tested by pulsed, pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. The power dissipation is limited by 150 °C junction temperature.
4. The min. value is 100% EAS tested guarantee.
5. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.

7. Typical operating characteristics

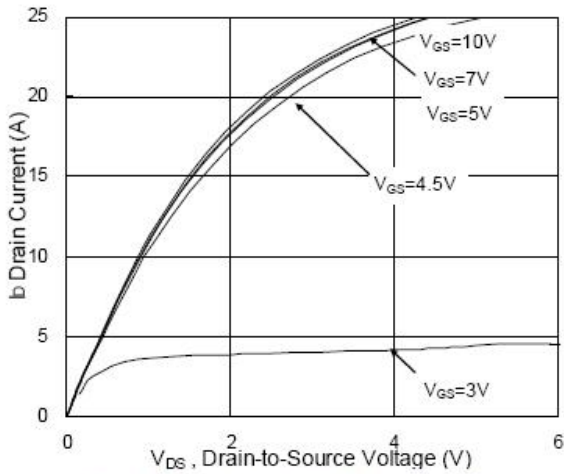


Fig.1 Typical output characteristics

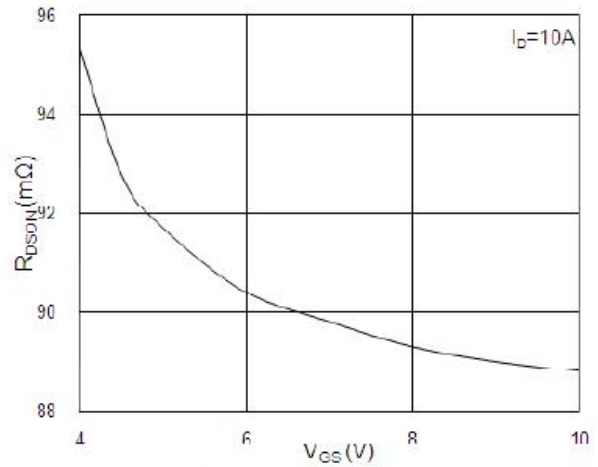


Fig.2 On-resistance vs. Gate-source

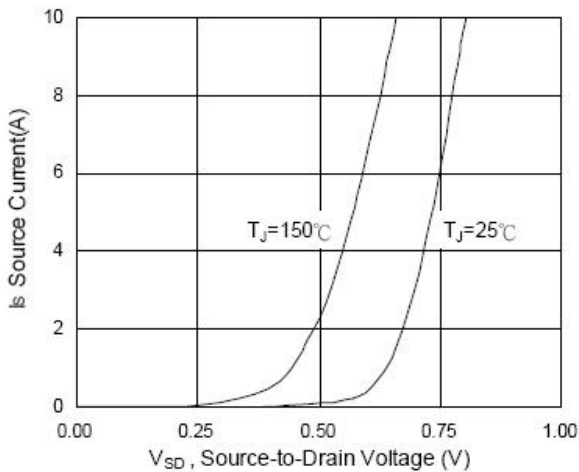


Fig.3 Forward characteristics of reverse

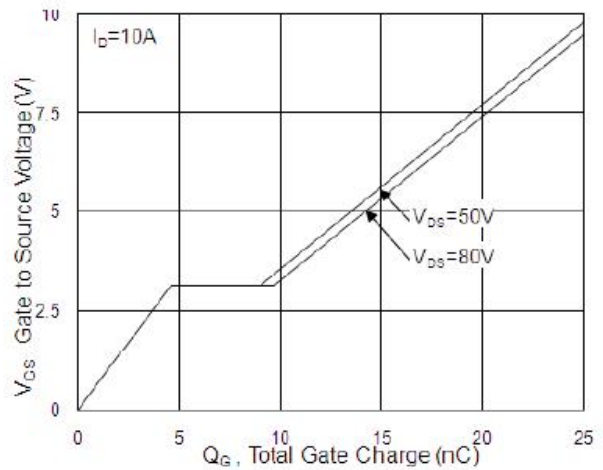


Fig.4 Gate-charge characteristics

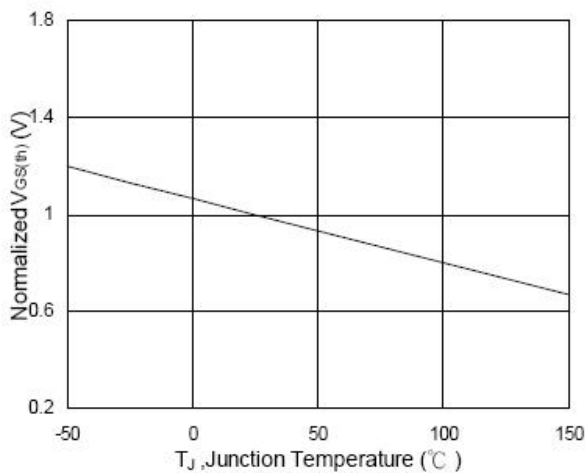


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

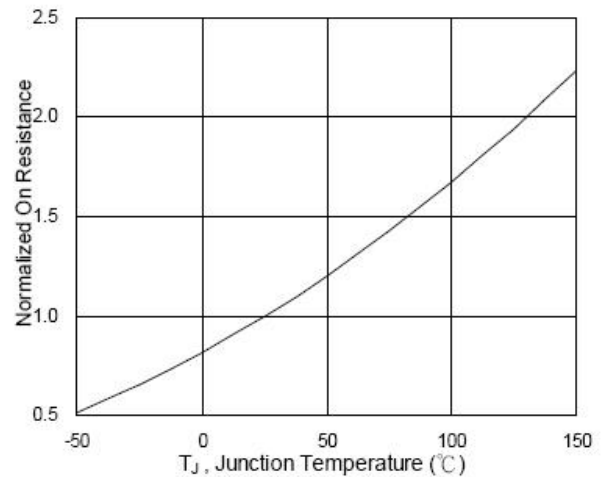


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

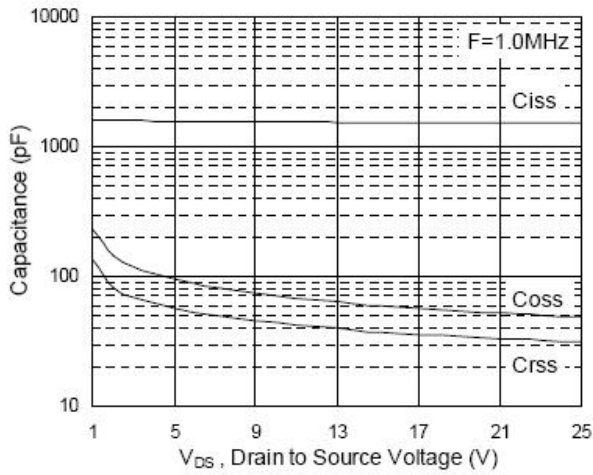


Fig.7 Capacitance

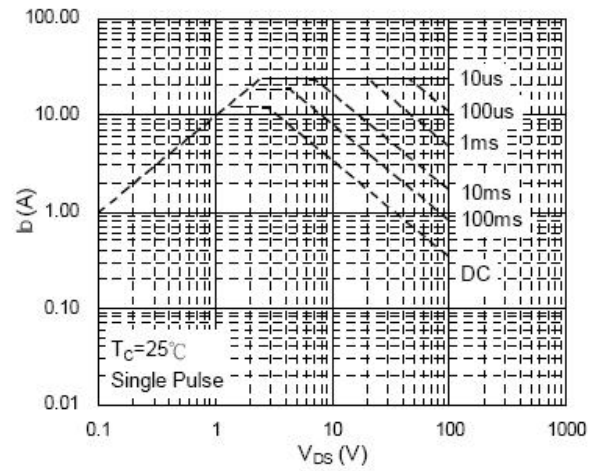


Fig.8 Safe operating area

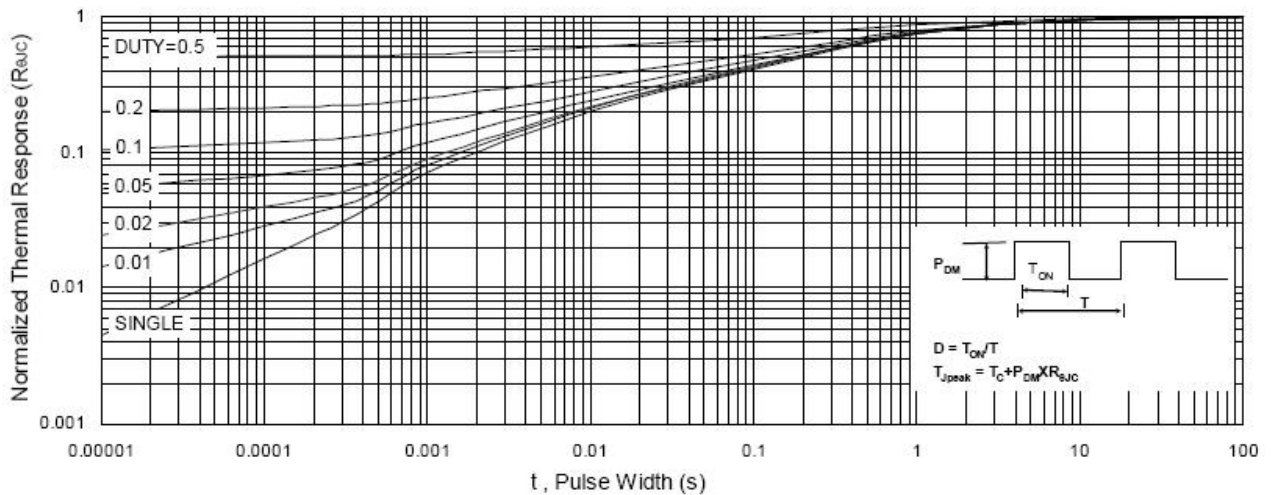


Fig.9 Normalized maximum transient thermal impedance

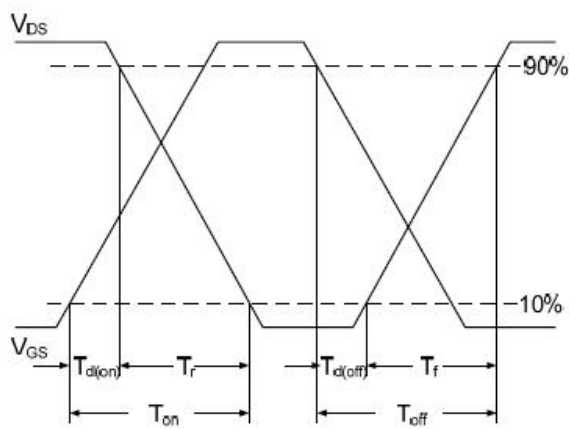


Fig.10 Switching time waveform

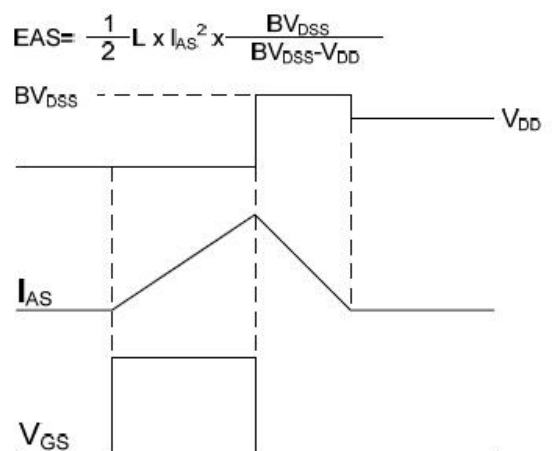


Fig.11 Gate charge waveform